REMARKS

Claims 1, 3-5 and 7-20 are pending in the application. Claims 9-14 and 20 stand withdrawn. Claims 1, 3-5, 7, 8, and 15-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Montague (US 5798283) in view of Kim (US 6500763) and Lee (US 6160314). Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Montague/Kim/Lee in view of Fladre (US 200410152272).

Claim Rejections -- 35 U.S.C. § 103(a)

As will be shown below, a prima facie case of obviousness has not be made for any of the pending claims of the subject application. The examiner is requested to provide the factual basis for the motivation or suggestion to combine the secondary references with the primary reference to achieve the claimed embodiments of the invention. Absent such factual support, the examiner must withdraw the rejections.

Claims 1, 3-5, 7, 8, and 15-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Montague (US 5798283) in view of Kim (US 6500763) and Lee (US 6160314).

Claim 1 is directed to a method of forming a surface micromachined MEMS device having both circuitry and structure. Among other things, claim 1 requires "depositing a conductive path directly on an oxide" that was applied to a substrate. This conductive path connects between the circuitry and structure. In contrast, Montague '283 does not teach such a process. Instead, the Montague reference teaches depositing polysilicon

on a nitride layer. In particular, as shown in Figure 1 and col. 5, lines 30-35 of Montague, Montague's MEMS device has a doped polysilicon layer 24 (a conductive path) on a nitride layer 22.

Lee '314 teaches use of a complex structure as a polishing stop for fabricating a semiconductor device. This structure is shown in fig. 2A of Lee:

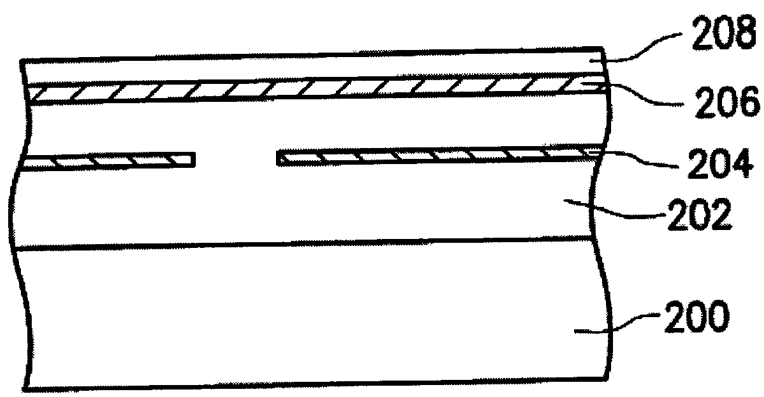

FIG. 2A

Lee describes the structure thusly:

"Referring first to FIG. 2A, a first dielectric layer 202 is formed on a semiconductor substrate 200. The dielectric layer 202, for example, is a silicon dioxide layer. An etching stop layer 204, for example, a silicon nitride layer, is formed in the dielectric layer 202.

> The materials of the polishing stop layer 206 and the dielectric layer 202 are different. A polishing stop layer 206 is formed on the dielectric layer 202. The material of the polishing stop layer 206 is, for example, silicon-oxy-nitride, silicon nitride or aluminum oxide, which are not easily removed by CMP and have a high polishing selectivity. The dielectric layer 202 is therefore more easily removed by chemical mechanical polishing than the polishing stop layer 206. A second dielectric layer 208 is formed on the polishing stop layer 206. The material of the second dielectric layer is different from the polishing stop layer 206, for example, silicon dioxide." See Lee '314, col. 2 lines 47 to 62.

To provide a motivation or a suggestion to replace Montague's nitride layer 22 with an oxide layer, a reference would need to teach that the materials are <u>fully</u> equivalent in layer 22 in Montague's application. Lee never describes nitride and oxide as interchangeable substitutes when used as a singular insulating layer over a semiconductor substrate. This is the function performed by Montague's layer 22. Instead, Lee mentions that in a layer of the complex sandwich shown in fig. 2A (layer 206), one or more materials would work. Performance as a polishing stop or etch stop is but one attribute of Montague's insulating layer 22. A reference would need to teach equivalence of all pertinent properties of the two materials in Montague's application to provide a suggestion to replace nitride with oxide – such as dielectric constant, etc. Lee '314 lacks such a teaching. Since Lee does not teach that oxide and nitride have fully equivalent properties for Montague's nitride insulating layer 22, a suggestion or motivation to combine Lee' '314 teachings with Montague's teaching is lacking and claim 1 is deemed non-obvious over Montague in view of Lee.

Kim '763 teaches a method for manufacturing an electrode of a

capacitor.

FIG. 1

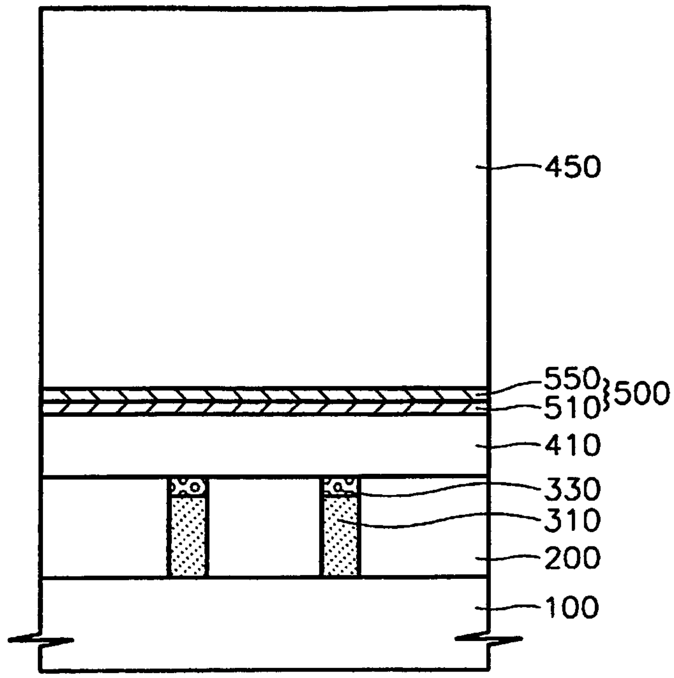

Fig. 1 of Kim '763 shows the structure formed by Kim's process.

Kim describes the process, thus:

"In a first embodiment of the present invention, FIG. 1 schematically illustrates a process of forming an etch stop layer 500 and a mold sacrificial insulating layer 450 on a **semiconductor substrate 100**. More specifically, a conductive plug 310, which will be electrically connected to a storage node, is formed on the semiconductor substrate 100 using a standard buried contact process. The conductive plug 310 is surrounded by a lower insulating layer 200 so that the **conductive plug 310** may be insulated from other conductive patterns (not shown) such as gates, which are formed on the semiconductor substrate 100, while the conductive plug 310 is electrically connected to an active region in the semiconductor substrate 100. Put another way, the conductive plug 310 functions as a buried contact. The thickness of the lower insulating layer 200 varies with necessity, but may be about 4000-5000 .ANG. depending on the thickness of the conductive plug 310.

The conductive plug 310 may be formed of various conductive materials, for example, conductive polysilicon. The conductive plug may be covered with a diffusion barrier layer 330. The diffusion barrier layer 330 may include an ohmic layer to serve as an ohmic

contact.

On the semiconductor substrate 100 having topology as a result of forming such various patterns, a support insulating layer 410 is formed. The support insulating layer 410 serves to support a three-dimensional storage node so that the storage node does not fall down or collapse. The support insulating layer 410 may be formed of an insulating material, which is usually used when a semiconductor device is manufactured. For example, the support insulating layer 410 may be formed by depositing a silicon oxide (SiO.sub.2) layer on the lower insulating layer 200 such that the conductive plug 310 is covered with the silicon oxide layer. The support insulating layer 410 must be formed to at least a minimum thickness for supporting a storage node. It is preferable that the support insulating layer 410 is formed to a thickness of about 2000-3000 .ANG.

Thereafter, the **etch stop layer 500**, which will be used in a later etching process, is formed on the support insulating layer 410. In one embodiment of the present invention, the etch stop layer 500 includes a tantalum oxide layer 510. For example, the tantalum oxide layer 510 is formed of ditantalum pentaoxide (Ta.sub.2 O.sub.5) on the support insulating layer 410 by sputtering or chemical vapor deposition (CVD). The tantalum oxide layer 510 is preferably formed to at least the minimum thickness needed to stop etching. For example, the thickness of the tantalum layer 510 may be about 10-90 .ANG., but may vary depending on a later etching process." See Kim '763, col. 3, line 31 to col. 4, line 19, emphasis added.

Thus, in Kim '763, conductor 310 lies between substrate 100 and the etch stop layer 500. While Kim may teach that in Kim's specific complex semiconductor structure, the etch stop layer may either be a nitride or an oxide, one of skill in this art could not infer from this teaching that Montague's insulating layer 22 can be either a nitride or an oxide. Montague's insulating layer 22 lies between the conductive path and the substrate and serves additional functions as compared to Kim's etch stop layer 500. Equivalence of materials can only be inferred from consideration of all relevant properties of the materials. Kim '763 like Lee '314 cannot serve as motivation or a suggestion to replace Montague's insulating layer with an "all oxide" layer since there is no teaching in Kim that the oxide would perform equally well or better than the nitride in

Montague's device structure. Thus, claim 1 is deemed non-obvious over Montague in view of Kim '763.

Since claim 1 is allowable over the cited art, claims 3-5, 7 and 8, which depend from claim 1 and add further limitations are also allowable for at least the same reasons as for claim 1. Claim 15 and dependent claims 16-18 are also allowable for the same reasons as for claim 1.

Claim Rejections -- 35 U.S.C. § 103(a)

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Montague/Kim/Lee in view of Fladre (US 200410152272).

The rejection for obviousness relies on Montague/Kim/Lee for teaching the limitations of claim 15, from which claim 19 depends. As shown above, Montague does not teach all of the limitations of claim 15. Fladre, likewise, does not provide the teaching, lacking in Montague/Kim/Lee, of a conductive path layered directly on an oxide. Since neither Montague/Kim/Lee nor Fladre teaches or suggests this required limitation of claim 19, claim 19 cannot be obvious over any combination of the two references.

The Commissioner is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 19-4972. Applicants request reconsideration of the rejected claims and a notice of allowance. The Examiner is requested to telephone the undersigned if any matters

remain outstanding so that they may be resolved expeditiously.

Respectfully submitted,

John L. Conway
Registration No. 48,241
Attorney for Applicants

Bromberg & Sunstein LLP
125 Summer Street
Boston, MA 02110-1618
(617) 443-9292

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